2827

Practitioner's Docket No. 6521-3-1-PCT-US *PATENT*

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Anthony A. Anthony, William M. Anthony

Application No.: 09/647,648
Filed: November 17, 2000
For: COMPONENT CARRIER

Group No.: 2827
Examiner: Norris, J.

Commissioner for Patents
Washington D.C. 20231

NOTIFICATION TO EXAMINER WITH REGARD TO POSSIBLE INTERFERENCE IN RELATED FILE

1. Transmitted herewith is a Notice to Examiner with Regard to Possible Interference in Related File for this application.

STATUS

2. Applicant is other than a small entity.

FEE DEFICIENCY

3. If an additional extension and/or fee is required, charge Account No. 15-0450.

Date: November 12, 2002

Signature of Practitioner

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CERTIFICATION UNDER 37 C.F.R. §§ 1.8(a) and 1.10*

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Anthony, A. et al.	**Examiner:**	Norris, J.
Serial No.:	09/647,648	**Art Unit:**	2827
Filed:	November 17, 2000	**Date:**	November 12, 2002
For:	COMPONENT CARRIER		

Commissioner of Patents and Trademarks
Washington, D.C. 20231

NOTICE TO EXAMINER WITH REGARD TO POSSIBLE INTERFERENCE IN RELATED FILE

This paper is not filed in response to any paper from the United State Patent Office. This paper is filed to provide notice that the applicant has filed a continuation-in-part application based on the present application in an attempt to provoke an interference with another application. Accordingly, no fees are believed to be due. If any additional fees are required, please consider this a petition for payment of them and charge them to Deposit Account 15-0450.

REMARKS

An Ex Parte Quayle Action mailed on September 24, 2002, has been received from the Examiner.

PENDING CONTINUATION-IN-PART APPLICATION TO PROVOKE INTERFERENCE

The applicant filed a continuation-in-part application serial number 10/237,079 on September 9, 2002, entitled "Universal Energy Conditioning Interposer with Circuit Architecture" naming Anthony et al. as inventors. That application claims priority to the following applications:

09/632,048 filed 08/03/00, which is a CIP of
09/594,447 filed 06/15/00, which is a CIP of
09/579,606 filed 05/26/00, which is a CIP of
09/460,218 filed 12/13/99, which is a continuation of
09/056,379, filed 04/07/98, now Patent No. 6,018,448, which is a CIP of
09/008,769, filed 01/19/98, now Patent No. 6,097,581, which is a CIP of
08/841,940, filed 04/08/97, now Patent No. 5,909,350

and ...

09/632,048 filed 08/03/00 which is also a CIP of
09/600,530 filed 07/18/00, which is a national stage application of
PCT/US99/01040 filed 01/16/99, which claims priority back to
09/008,769, filed 01/19/98, now Patent No. 6,097,581.

In the continuation-in-part application serial number 10/237,079 filed September 9, 2002, the applicant copied claims from 1-30 from the publication WO 02/27794 A2 of application serial number PCT/US01/30295, filed September 27, 2001, which claims priority to United States application serial number 09/675,789, filed September 29, 2000. A copy of the claims 1-30 are attached for your reference. The applicant copied claims to provoke an interference with application serial no. 09/675,789 or any continuation or division thereof claiming the same patentable invention.

The present application serial number 09/647,648 is related to the continuation-in-part application serial number 10/237,079 filed September 9, 2002. Therefore, if an interference is declared and, if the Examiner deems the claims in the present application to be patentably indistinct from the claims involved in the interference, the Examiner should proceed to examine the present application in accordance with MPEP 2315.01. Note that patentable indistinctness currently requires a showing of two-way obviousness. See Winter v. Fujita, 53 USPQ2d 1234 (PTOBPAI 1999)(expanded panel consisting of Stoner, CAPJ, McKelvey, SAPJ, Schafer, Lee, and Torczon, APJs)(opinion by SAPJ McKelvey). If the Examiner does not deem the claims in

this application to be patentably indistinct from the claims involved in the interference, then the interference should not affect prosecution of this application.

If the Examiner should have any question regarding this application or the notice, a call to Applicant's attorney would be appreciated.

Respectfully submitted,
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Attorney Docket No.: **6521-3-1-PCT-US**

CLAIMS

What is claimed is:

1. An integral capacitor comprising:

a power plane having a power surface and a power periphery, the power plane coupling power to signals of an integrated circuit operating at a fundamental frequency;

a first ground plane having a first ground surface and a first ground periphery, the first ground plane coupling ground to the signals, the first ground plane being separated from the power plane by a first distance, the first ground surface being larger than the power surface and the first ground periphery extending at least a second distance from the power periphery, the second distance being at least larger than N times the first distance; and

a dielectric layer formed between the power plane and the first ground plane.

2. The integral capacitor of claim 1 further comprising:

a second ground plane having a second ground surface and a second ground periphery, the second ground plane being separated from the power plane by the third distance, the second ground surface being larger than the power surface and the second ground periphery extending at least a fourth distance from the power periphery, the fourth distance being at least larger than M times the third distance, the second ground plane being coupled to the first ground plane by a via chain connecting a first plurality of vias located around the first ground periphery to a second plurality of vias located around the second ground periphery, the first and second pluralities of vias having adjacent vias, the

adjacent vias being spaced apart by a via distance that is smaller than a quarter wavelength of the fundamental frequency.

3. The integral capacitor of claim 2 wherein the dielectric layer is made of a dielectric material having a high dielectric constant.

4. The integral capacitor of claim 1 wherein N is an integer ranging from 1 to 20.

5. The integral capacitor of claim 1 wherein M is an integer ranging from 1 to 20.

6. The integral capacitor of claim 1 wherein the first plurality of vias having electrical contact to a plurality of adjacent contacts, the adjacent contacts being spaced apart by a contact distance that is smaller than a quarter wavelength of the fundamental frequency.

7. The integral capacitor of claim 6 wherein the contacts are ones of controlled collapse chip connection (C4) bumps, ball grid array (BGA) balls, and **flip** chip pin grid array (FCPGA) pins.

8. The integral capacitor of claim 1 further comprises a contact array to connect to at least the first ground plane and the power plane.

9. The integral capacitor of claim 8 wherein the contact array is one of a C4 bump array, a BGA ball array, and a FCPGA pin array.

10. The integral capacitor of claim 9 wherein the ground plane has a plurality of adjacent contacts, the adjacent contacts being ones of controlled collapse chip connection (C4) bumps, ball grid array (BGA) balls, and flip chip pin grid array (FCPGA) pins and spaced apart by a contact distance that is smaller than a quarter wavelength of the fundamental frequency.

11. A packaged device comprising:

a die containing an integrated circuit;

a plurality of controlled collapse chip connection (C4) bumps attaching the die to a substrate; and

an integral capacitor attaching to the die to reduce radiation, the integral capacitor comprising:

a power plane having a power surface and a power periphery, the power plane coupling power to signals of an integrated circuit operating at a fundamental frequency,

a first ground plane having a first ground surface and a first ground periphery, the first ground plane coupling ground to the signals, the first ground plane being separated from the power plane by a first distance, the first ground surface being larger than the power surface and the first ground

periphery extending at least a second distance from the power periphery, the second distance being at least larger than N times the first distance, and

a dielectric layer formed between the power plane and the first ground plane.

12. The packaged device of claim 11 wherein the integral capacitor further comprising:

a second ground plane having a second ground surface and a second ground periphery, the second ground plane being separated from the power plane by the third distance, the second ground surface being larger than the power surface and the second ground periphery extending at least a fourth distance from the power periphery, the fourth distance being at least larger than M times the third distance, the second ground plane being coupled to the first ground plane by a via chain connecting a first plurality of vias located around the first ground periphery to a second plurality of vias located around the second ground periphery, the first and second pluralities of vias having adjacent vias, the adjacent vias being spaced apart by a via distance that is smaller than a quarter wavelength of the fundamental frequency.

13. The packaged device of claim 12 wherein the dielectric layer is made of a dielectric material having a high dielectric constant.

14. The packaged device of claim 11 wherein N is an integer ranging from 1 to 20.

15. The packaged device of claim 11 wherein M is an integer ranging from 1 to 20.

16. The packaged device of claim 11 wherein the first plurality of vias having electrical contact to a plurality of adjacent contacts, the adjacent contacts being spaced apart by a contact distance that is smaller than a quarter wavelength of the fundamental frequency.

17. The packaged device of claim 16 wherein the contacts are ones of controlled collapse chip connection (C4) bumps, ball grid array (BGA) balls, and flip chip pin grid array (FCPGA) pins.

18. The packaged device of claim 11 wherein the integral capacitor further comprises a contact array to connect to at least the first ground plane and the power plane.

19. The packaged device of claim 18 wherein the contact array is one of a C4 bump array, a BGA ball array, and a FCPGA pin array.

20. The packaged device of claim 19 wherein the ground plane has a plurality of adjacent contacts, the adjacent contacts being ones of controlled collapse chip connection (C4) bumps, ball grid array (BGA) balls, and flip chip pin grid array (FCPGA) pins and spaced apart by a contact distance that is smaller than a quarter wavelength of the fundamental frequency.

21. A method comprising:

coupling power to signals of an integrated circuit operating at a fundamental frequency by a power plane having a power surface and a power periphery;

coupling ground to the signals by a first ground plane having a first ground surface and a first ground periphery, the first ground plane being separated from the power plane by a first distance, the first ground surface being larger than the power surface and the first ground periphery extending at least a second distance from the power periphery, the second distance being at least larger than N times the first distance; and

forming a dielectric layer between the power plane and the first ground plane.

22. The method of claim 21 further comprising:

coupling a second ground plane to the first ground plane by a via chain, the second ground plane having a second ground surface and a second ground periphery, the second ground plane being separated from the power plane by the third distance, the second ground surface being larger than the power surface and the second ground periphery extending at least a fourth distance from the power periphery, the fourth distance being at least larger than M times the third distance, the via chain connecting a first plurality of vias located around the first ground periphery to a second plurality of vias located around the second ground periphery, the first and second pluralities of vias having adjacent vias, the adjacent vias being spaced apart by a via distance that is smaller than a quarter wavelength of the fundamental frequency.

23. The method of claim 22 wherein the dielectric layer is made of a dielectric material having a high dielectric constant.

24. The method of claim 21 wherein N is an integer ranging from 1 to 20.

25. The method of claim 21 wherein M is an integer ranging from 1 to 20.

26. The method of claim 21 wherein the first plurality of vias having electrical contact to a plurality of adjacent contacts, the adjacent contacts being spaced apart by a contact distance that is smaller than a quarter wavelength of the fundamental frequency.

27. The method of claim 26 wherein the contacts are ones of controlled collapse chip connection (C4) bumps, ball grid array (BGA) balls, and flip chip pin grid array (FCPGA) pins.

28. The method of claim 21 further comprises connecting to at least the first ground plane and the power plane by a contact array.

29. The method of claim 28 wherein the contact array is one of a C4 bump array, a BGA ball array, and a FCPGA pin array.

30. The method of claim 29 wherein the ground plane has a plurality of adjacent contacts, the adjacent contacts being ones of controlled collapse chip connection

(C4) bumps, ball grid array (BGA) balls, and flip chip pin grid array (FCPGA) pins and spaced apart by a contact distance that is smaller than a quarter wavelength of the fundamental frequency.

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